SEMICONDUCTOR MEMORY DEVICE WITH A DECOUPLING CAPACITOR

ABSTRACT

A semiconductor memory device includes a core block having sub-arrays and sense amplifier regions. First and second charge storing regions are disposed at sides of the core block. First and second decoupling capacitors are formed at the first and second charge storing regions, respectively. A plurality of first voltage supply lines are disposed to supply a power supply voltage to the sense amplifier regions and are connected to one electrode of each of the first and second decoupling capacitors. A plurality of second voltage supply lines are disposed to supply a ground voltage to the sense amplifier regions and are connected to the other electrode of each of the first and second decoupling capacitors.